WHAT IS CLAIMED IS:

1. An ink jet print head identification circuit, suitable for using in an ink jet printer that comprises a reset signal line, at least one clock signal line, and an identification code signal line, for identifying a type of the ink jet print head, comprising:

a counter, coupled to the reset signal line and at least one clock signal line, used to reset the counter when a reset signal is received from the reset signal line, and used to count a count value of the counter to next value when a corresponding clock signal is received from the at least one clock signal line, so as to output the count value from a plurality of output terminals of the counter;

a logic unit, comprising a plurality of input terminals and an output terminal, wherein the output terminal of the logic unit is coupled to the identification code signal line, so as to output an identification code that represents the type of the ink jet print head; and

a programming unit, coupled to the output terminals of the counter and the input terminals of the logic unit, used to program the corresponding connection between each output terminal of the counter and each input terminal of the logic unit.

2. The ink jet print head identification circuit of claim 1, wherein, after the counter is reset, the count value of the counter is counted in a sequence of 1, 2, 4, 8, 16, ..., etc.

3. The ink jet print head identification circuit of claim 1, wherein the logic unit is an OR gate, a NAND gate, or a decoder.

4. The ink jet print head identification circuit of claim 1, wherein the logic unit further comprises an enabling control terminal, and the enabling control terminal is coupled to a clock signal line.

5. The ink jet print head identification circuit of claim 1, wherein the programming unit is programmed in a mask programmed way when the identification circuit of the ink jet print head is being manufactured, so as to store the identification code.

6. The ink jet print head identification circuit of claim 1, wherein the programmable programming unit is provided by using a plurality of fuses, so as to store the identification code.

7. The ink jet print head identification circuit of claim 1, wherein the programmable programming unit is provided by using a plurality of electrical connectors, so as to store the identification code.

8. An ink jet print head identification circuit, suitable for use in an ink jet printer that comprises a reset signal line, at least one clock signal line, and an identification code signal line, for identifying a type of the ink jet print head, comprising:

a counter, coupled to the reset signal line and at least one clock signal line, used to reset the counter when a reset signal is received from the reset signal line, and used to count a count value of the counter to next value when a corresponding clock signal is received from the at least one clock signal line, so as to output the count value from a plurality of output terminals of the counter;

a plurality of switches, wherein each of the plurality of switches comprises an input terminal, an output terminal, and a control terminal, and all output terminals of the switches are coupled to the identification code signal line, so as to output an identification code that represents the type of the ink jet print head, and each control terminal of the switches is coupled to the corresponding output terminal of the counter, respectively; and

a programming unit, coupled to the input terminals of the switches, used to program the input value of the input terminal of the switches according to the identification code to be stored.

9. The ink jet print head identification circuit of claim 7, wherein, after the counter is reset, the count value of the counter is counted in a sequence of 1, 2, 4, 8, 16, ..., etc.

10. The ink jet print head identification circuit of claim 7, wherein the switches are a plurality of NMOS transistors or a plurality of CMOS transistors.

11. The ink jet print head identification circuit of claim 7, wherein the programming unit is programmed in a mask programmed way when the identification circuit of the ink jet print head is being manufactured, so as to store the identification code.

12. The ink jet print head identification circuit of claim 7, wherein the programmable programming unit is provided by using a plurality of fuses, so as to store the identification code.

13. The ink jet print head identification circuit of claim 7, wherein the programmable programming unit is provided by using a plurality of electrical connectors, so as to store the identification code.

14. An ink jet print head identification method, suitable for identifying a type of the ink jet print head, comprising:

providing a reset signal and at least one clock signal;

resetting a count value when the reset signal is received;

counting the count value to next value when the at least one clock signal is received; and

programming a logic unit according to an identification code that represents the type of the ink jet print head and the count value, so that the ink jet print head sequentially outputs the identification code.

15. The ink jet print head identification method of claim 12, wherein, after the counter is reset, the count value of the counter is counted in a sequence of 1, 2, 4, 8, 16, ..., etc.

16. The ink jet print head identification method of claim 12, wherein the logic unit is an OR gate, a NAND gate, or a decoder.

17. The ink jet print head identification method of claim 12, wherein the logic circuit is a plurality of NMOS transistors or a plurality of CMOS transistors.